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### Re: Atmel ARM7 to **DRAM** interface

... Do not forget to 'wake-up' **DRAM**, holding CAS# high several hundred ms at ... I have implemented a generic **SDRAM controller**; it fits into 29 PLD macrocells (Altera ... [comp.arch.embedded](#) - Nov 11, 2001 by ikauranen - [View Thread \(5 articles\)](#)

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### Re: Why does 32-bit give a performance hit?

... far, 3dfx seems to have the simplest memory **controller** which explains ... with the fastest possible SRAM or DDR **SDRAM** (or better yet on chip **embedded DRAM**). ... [comp.sys.ibm.pc.hardware.video](#) - May 12, 1999 by Salim Qadri - [View Thread \(8 articles\)](#)

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### Re: Have DDR graphics cards reached their memory bandwidth limit ...

... a long ways to go (and other designs, most notably **embedded DRAM**, may end ... **SDRAM** interface, so for these companies to produce a DDR **SDRAM controller** is probably ... [comp.sys.ibm.pc.hardware.chips](#) - Sep 24, 2000 by Anthony Hill - [View Thread \(27 articles\)](#)

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### Re: Using **DRAM** SIMMs w/ MCUs

[comp.arch.embedded](#) - Aug 30, 2002 by Jack Klein - [View Thread \(12 articles\)](#)

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### Re: **SDRAM** Access from a Microcontroller?

... I've designed with both, and **DRAM** is significantly easier than **SDRAM**. ... If I were you, I'd search for an **SDRAM controller** with a simple **controller** interface. ... [comp.arch.embedded](#) - Jan 23, 2002 by Howard Delman - [View Thread \(19 articles\)](#)

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### Re: **Embedded** Microprocessor w/Ethernet

... logic includes an interrupt **controller**, **DRAM/ SDRAM controller**, and a ... arbiter and an external memory **controller**. ... [www.redhat.com/embedded/technologies/redboot](#) ... [comp.dcom.lans.ethernet](#) - Jun 21, 2002 by Dainis Strupis - [View Thread \(3 articles\)](#)

#### [Embedded DRAM & SRAM](#)

A Technical Analysis of Market, Technology, Design & Apps Trends  
[www.memorystrategies.com](#)  
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### Re: How to keep **DRAM** content over reset on x86 (Northbridge/ ...

... auto-refresh is used, where a RAS before CAS access is generated by the **SDRAM controller**.

When a PC notebook go into standby mode/wakeup, the **DRAM** content is ...  
[comp.arch](#) - Nov 4, 2002 by Konrad Schwarz - [View Thread \(28 articles\)](#)

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... I have used to design a video ASIC chip with **DRAM & SDRAM controller**. Another problem is the cost. ... Besides, it has some **embedded** chip for FPGAs. ...  
[comp.lang.vhdl](#) - Apr 22, 1998 by leslie.yip@asmpt.com - [View Thread \(8 articles\)](#)

[Questions about Coldfire MC5307 SDRAM controller and interface to ...](#)


Referring to the **SDRAM Controller** section in the updated Users ... the **SDRAM** Clock, interface signals to the **SDRAM** will change on the rising edge of the **DRAM** clock ...  
[comp.arch.embedded](#) - Feb 8, 2000 by usenet201@hotmail.com - [View Thread \(2 articles\)](#)

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